What is Claimed is

1. A method of manufacturing a semiconductor device, said semiconductor device comprising a first conduction type thin film transistor and a second conduction type thin film transistor, said method comprising:

providing a substrate having a first area and a second area;

forming a gate dielectric layer on said substrate;

forming a conductive layer on said gate dielectric layer;

selectively removing a portion of said conductive layer to form a first gate electrode on said gate dielectric layer corresponding to said first area and a portion of remains of said conductive layer substantially overlying said second area;

doping a first impurity of a first conduction type in said first area;

forming a spacer on a sidewall of said first gate electrode;

doping a second impurity of said first conduction type in said first area to form said first conduction type thin film transistor;

removing a portion of said conductive layer corresponding to said second area to form a second gate electrode on said gate dielectric layer corresponding to said second area; and

doping an impurity of a second conduction type in said second area to form said second conduction type thin film transistor.

2. The method of claim 1, wherein said step of selectively removing said conductive layer to form said first gate electrode comprises:

forming a photoresist layer on said conductive layer;

patterning said photoresist layer so that said photoresist layer defines said first gate electrode of said conductive layer corresponding to said first area; and

etching said conductive layer to expose said gate dielectric layer using said

photoresist layer as a mask, so that a first portion of said conductive layer forms said first gate electrode, and a second portion of said conductive layer substantially overlies said second area.

3. The method of claim 1, wherein said step of doping said first impurity of said first conduction type comprises a step of ion implanting a fist n-type dopant into said first area to form at least one lightly doped region by using said first gate electrode as a mask.

4. The method of claim 3, wherein said step of doping said second impurity of said first conduction type comprises a step of ion implanting a second n-type dopant into said first area to form at least one heavy doped region by using said first gate electrode and said spacer as a mask, and wherein said heavy doped region overlaps a portion of said lightly doped region.

5. The method of claim 1, wherein said first and said second impurities of said first conduction type are two different or same doping materials.

6. The method of claim 5, wherein said impurity of said second conduction type comprises a p-type dopant.

7. The method of claim 5, wherein said step of doping said impurity of said second conduction type comprises a step of ion implanting a p-type dopant into said second area to form at least one doped region by using said patterned photoresist layer as a mask.

8. The method of claim 1, wherein said step of forming said spacer comprises:

forming a conformal dielectric layer over said semiconductor substrate; and

anisotropically etching said conformal dielectric layer to form said spacer on said sidewall of said first gate electrode.

9. The method of claim 1, wherein said gate dielectric layer is selected from the group

consisting of a nitride layer, an oxide layer, and a combination thereof.

10. A method of manufacturing a semiconductor device, said semiconductor device comprising an n-type thin film transistor and a p-type thin film transistor, said method comprising:

providing a substrate having a first area and a second area;

forming a gate dielectric layer on said substrate;

forming a conductive layer on said gate dielectric layer;

selectively removing a portion of said conductive layer, so that a first portion of said conductive layer forms a first gate electrode on said gate dielectric layer corresponding to said first area, and a second portion of said conductive layer substantially over said second area;

ion implanting a first n-type dopant into said first area to form a lightly doped region by using said first gate electrode as a mask;

forming a conformal dielectric layer over said semiconductor substrate;

etching said conformal dielectric layer to form a spacer on a sidewall of said first gate electrode;

ion implanting a n-type dopant into said first area to form a heavy doped region by using said spacer and said first gate electrode as a mask, said heavy doped region overlapping a portion of said lightly doped region to form said n-type thin film transistor with said lightly doped region;

removing a portion of said second portion of said conductive layer to form a second gate electrode on said gate dielectric layer corresponding to said second area; and

ion implanting a p-type dopant into said second area by using said patterned photoresist layer as a mask to form said p-type transistor.

11. The method of claim 10, wherein said first n-type dopant and said second n-type dopant are two different doping materials.

12. The method of claim 10, wherein said first n-type dopant and said second n-type dopant are the same doping materials.

13. The method of claim 10, wherein said gate dielectric layer is selected from the group consisting of a nitride layer, an oxide layer, and a combination thereof.

14. A semiconductor device with a lightly doped region, comprising:

a substrate having a first area and a second area;

a first type thin film transistor formed in said first area; and

a second type thin film transistor formed in said second area;

wherein said first type thin film transistor comprises:

first source/drain regions formed in said substrate and separated by a first channel;

a first gate dielectric layer formed on said substrate covering said first channel;

a first gate electrode formed on said first gate dielectric layer corresponding to said first channel;

a spacer formed on a sidewall of said first gate electrode; and a lightly doped region formed in a portion of said source/drain region corresponding to said spacer;

and wherein said second type thin film transistor comprises:

second source/drain regions formed in said substrate and separated by a second channel;

a second gate dielectric layer formed on said substrate covering said second channel; and

a second gate electrode formed on said second gate dielectric layer corresponding to said second channel.

15. The semiconductor device of claim 14, wherein said first and second type thin film transistors comprises an n-type and a p-type thin film transistors.

16. The semiconductor device of claim 14, wherein said first and second dielectric layers are selected from the group consisting of a nitride layer, an oxide layer, and a combination thereof.